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# MS-7636 mATX Version: 3.1



## CPU:

INTEL - Lynnfield/ Clarkdale LGA 1156

## Main Memory:

Dual Channel DDRIII **x 2 (Max 16GB) (800 / 1066 / 1333/ 1600\* / 1800\* / 2133\*MHz)**

## System Chipset:

South Bridge : INTEL IBEXPEAK PCH (H55)

## On Board Chip:

Super I/O : FINTEK F71889ED  
 LAN : Realtek RTL8111E  
 HD Audio : Realtek ALC887 **colay ALC892**

## Expansion Slots:

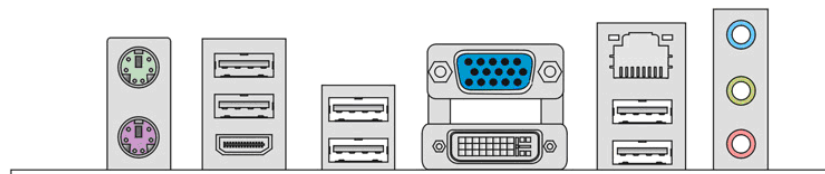
PCI-EPRESS X 16 SLOT **x 1**  
 PCI-EPRESS X 1 SLOT **x 2**

## PWM:

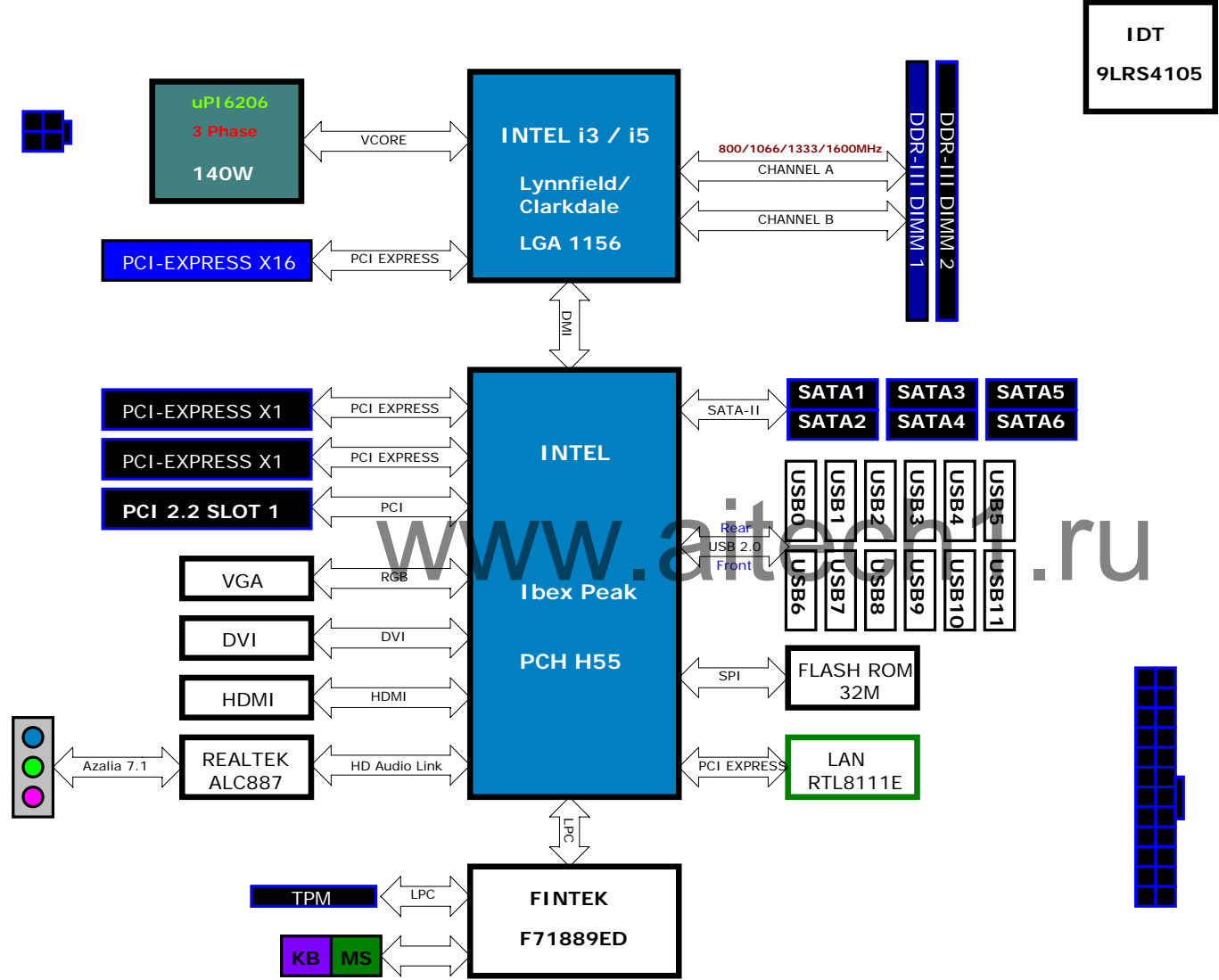
Controller : UPI uP6206 **(3 Phase / 125W)**

## Clock Generator:

Controller : IDT 9LRS4105

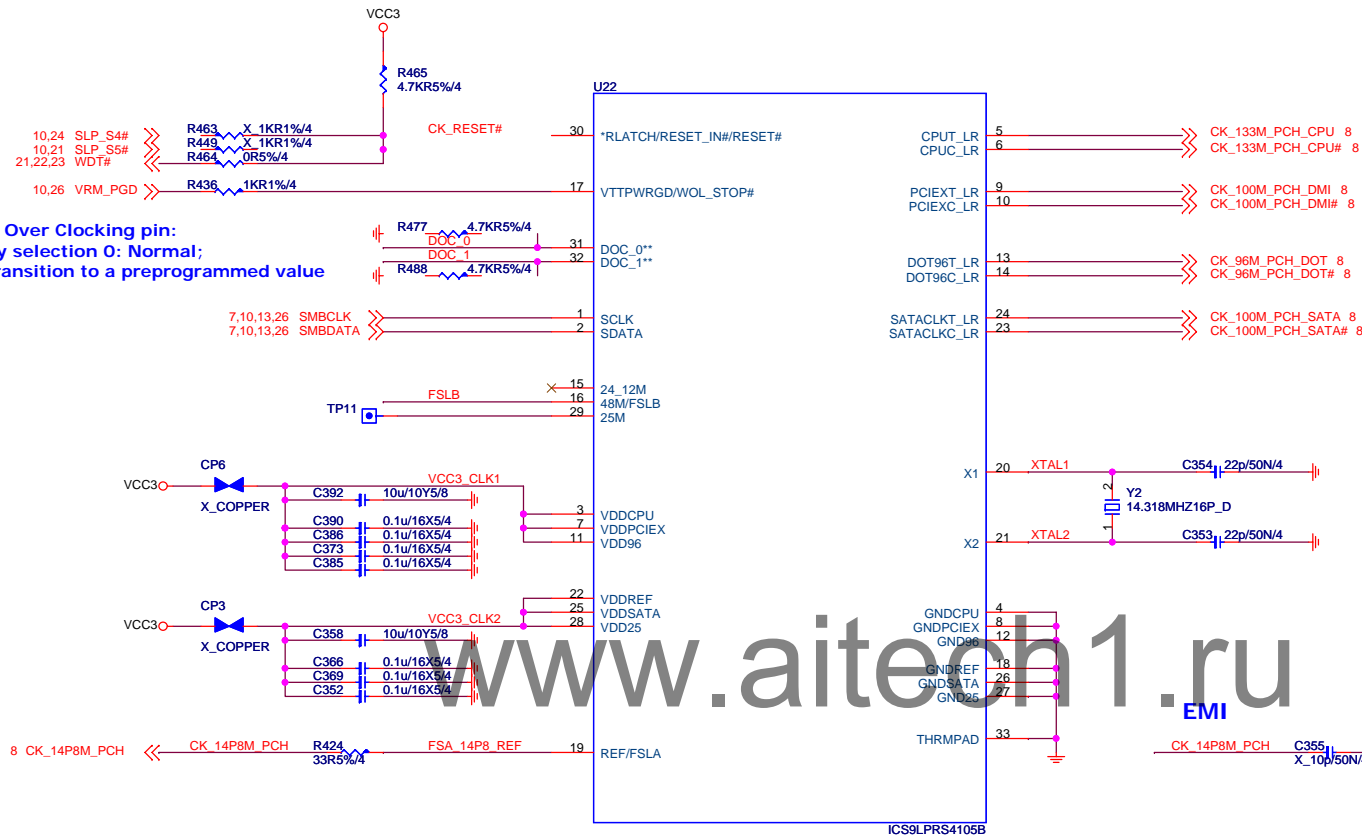


Block Diagram



Bom Config	Audio	LAN	USB1	JUSB2/ JUSB3	APS LED	OC SW	CAP
Cfg-7636-30_A	892 / 6 PORT JACK	8111E (Gb LAN)	Y	Y	N	N	OSCON
Cfg-7636-30_B	887 / 3 PORT JACK	8105E(10/100)	N	Y	N	N	OSCON+EL
Cfg-7636-30_C	887 / 3 PORT JACK	8111E (Gb LAN)	N	N	N	N	OSCON
Cfg-7636-30_D							

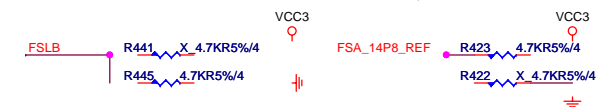
# CLK GEN ICS9LPRS4105B



**DOC\_0\*\*:**Dynamic Over Clocking pin:  
real time frequency selection 0: Normal;  
1: Frequency will transition to a preprogrammed value  
in the I2C.

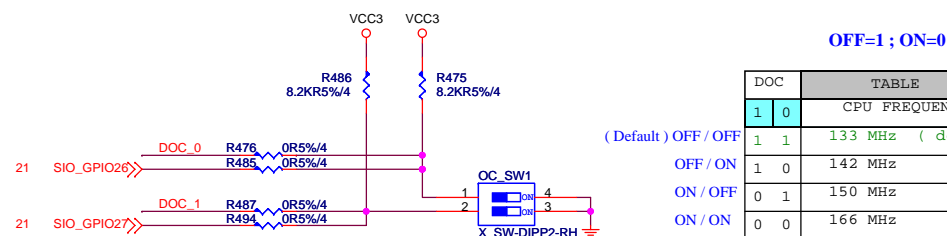
## CLOCK GEN STRAPING

FS4 B0b4	FS3 B0b3	FS2 B0b2	FSB B0b1	FSA B0b0	CPU Mhz	Spread %
0	0	0	0	0	100.00	-0.5
0	0	0	0	1	133.33	-0.5
0	0	0	1	0	200.00	-0.5
0	0	0	1	1	166.66	-0.5



Pin16: 48MHz clock output. / 3.3V tolerant input  
for CPU frequency selection. Low voltage  
threshold inputs, see input electrical  
characteristics for Vil\_FS and Vih\_FS values.

Pin19: 14.318 MHz reference clock./ 3.3V  
tolerant input for CPU frequency selection.  
Refer to input electrical characteristics for  
Vil FS and Vih FS values.



DOC		TABLE
1	0	CPU FREQUENCY
1	1	133 MHz ( default )
1	0	142 MHz
0	1	150 MHz
0	0	166 MHz

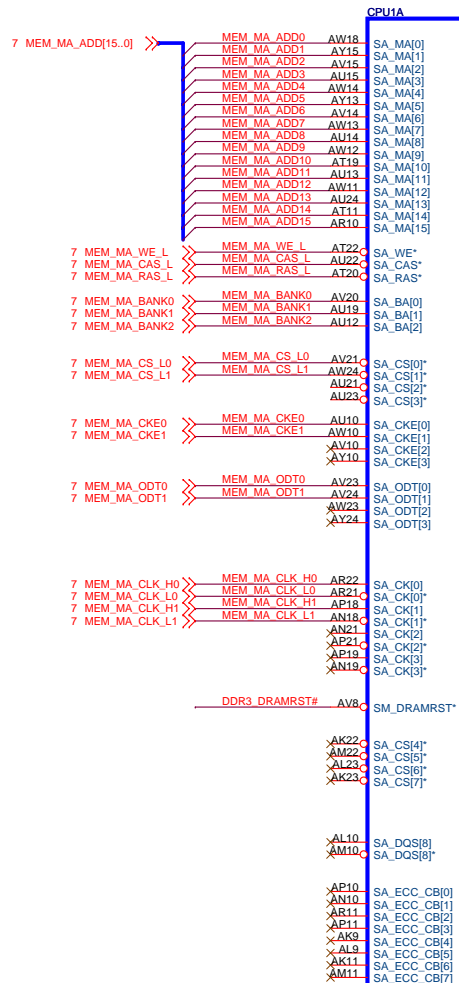


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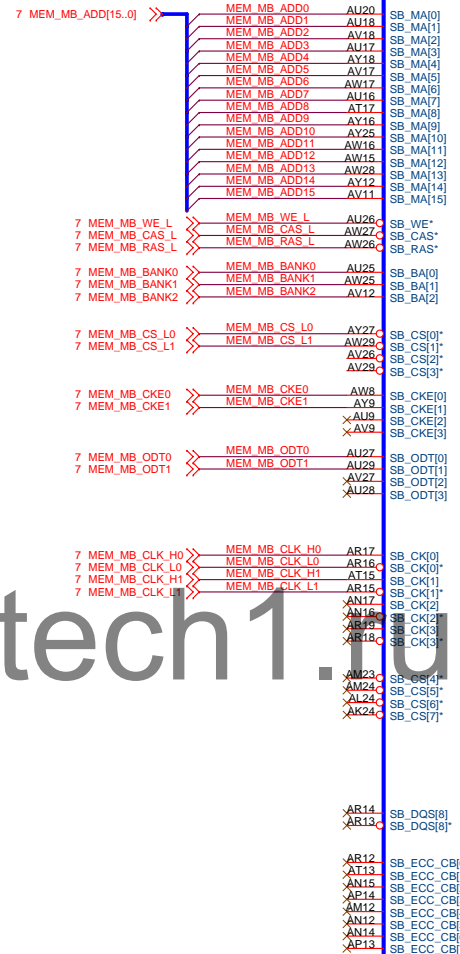
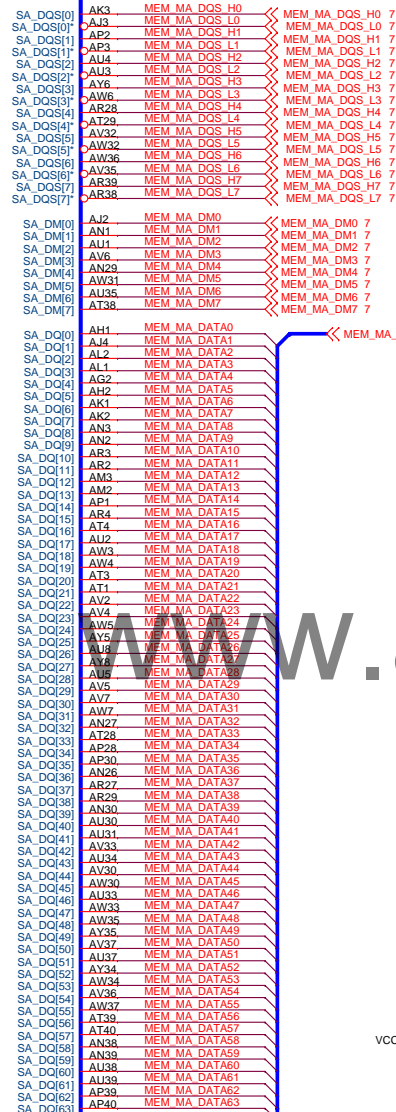
Size Custom	Document Description <b>CLK - ICS 9LRS4105B</b>	Rev 3.1
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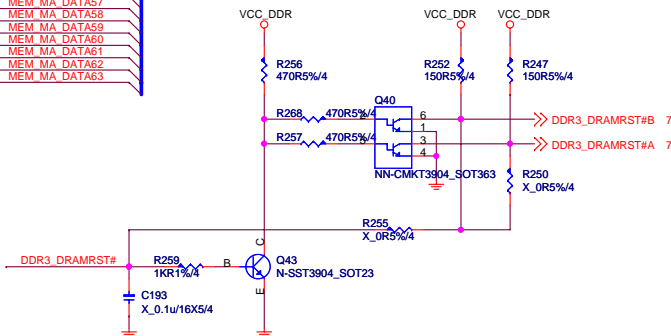
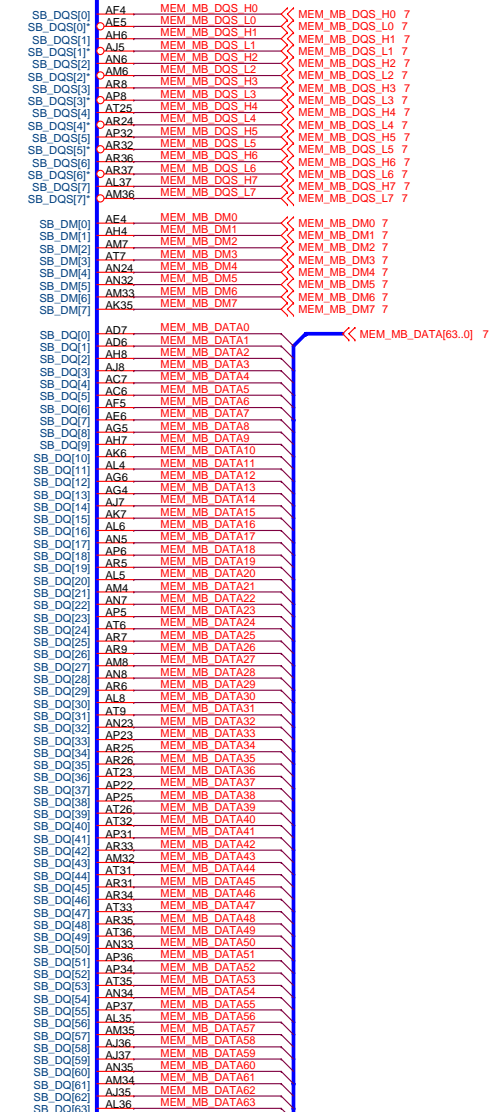
**DDR\_A**

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**DDR\_B**

2 OF 12



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**MS-7636**

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Custom	<b>CPU - MEM</b>	3.1
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1



1

1



1

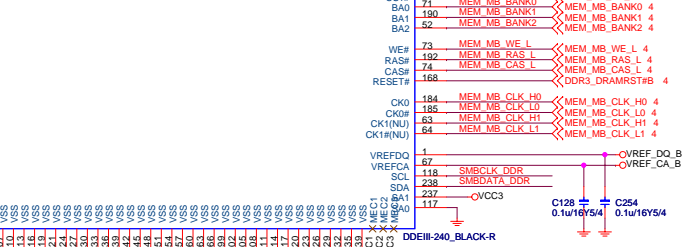
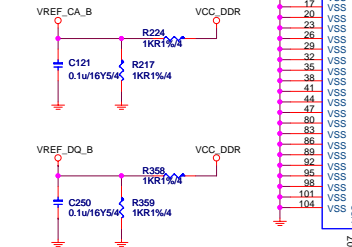
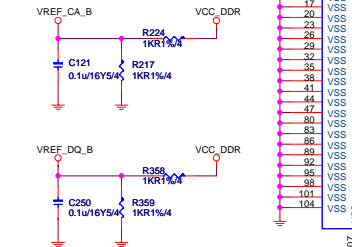
1

1

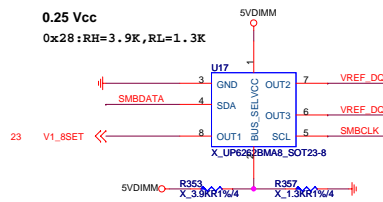
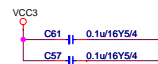
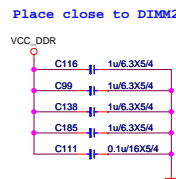





RESET#(Output) : A synchronously forces all registered output LOW when RESET# is LOW. This signal can be used by the design to ensure that CKE is LOW and DQs are High-Z.

**DDR**[illegible]

```
DIMM2 (CHANNEL-B)
ADDRESS = 1:0 [SA1:SA0]
```



Address	0x2A	0x28	0x26	0x24	0x22	0x20
R1 (kΩ)	open	3.9	3	2.2	1.3	10
R2 (kΩ)	10	1.3	2.3	3	3.9	open
BUS_SEL Voltage (% of VCC)	0	25	40	60	75	100



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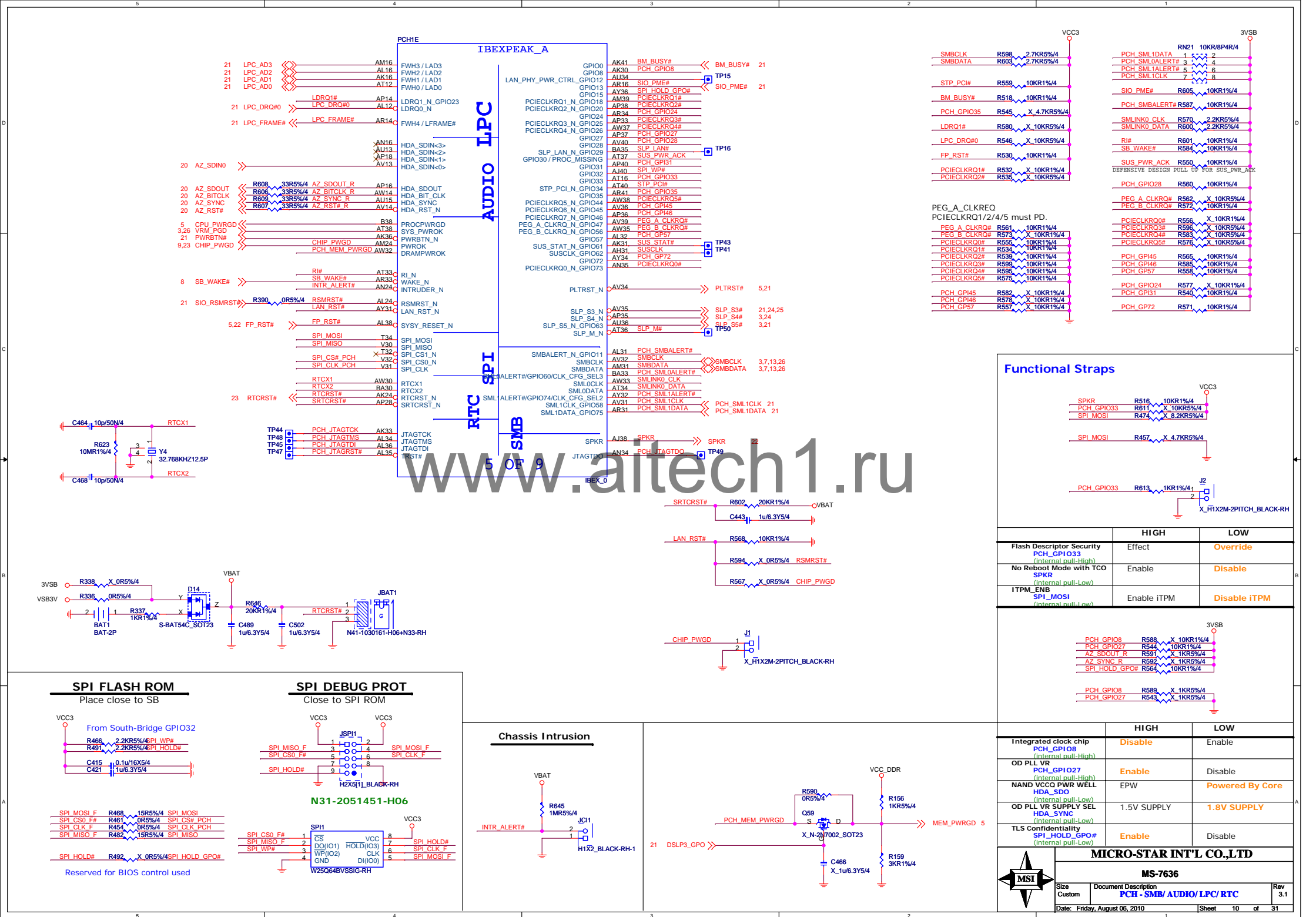
Size Custom	Document Description <b>DDR3 - DIMM1 / 2</b>	Rev 3.1
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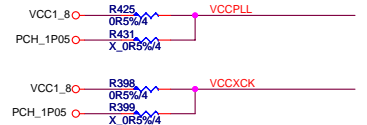
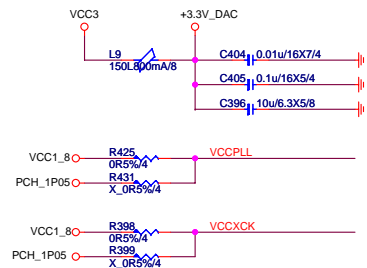
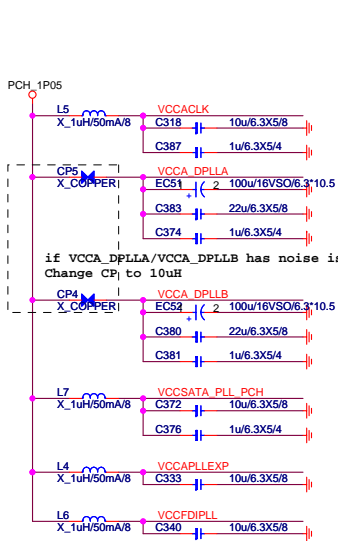






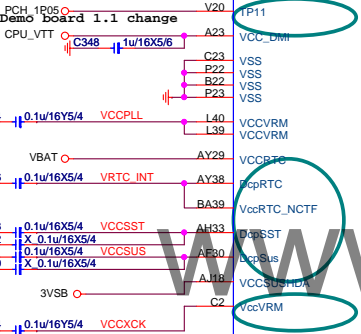
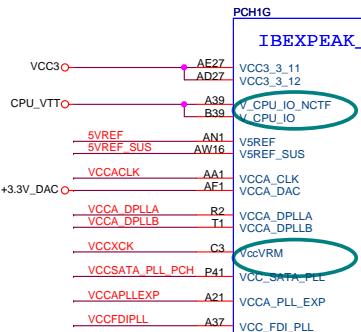
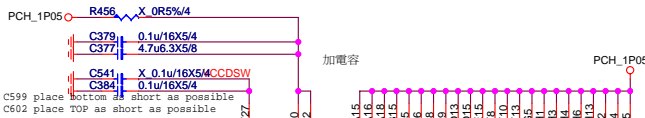
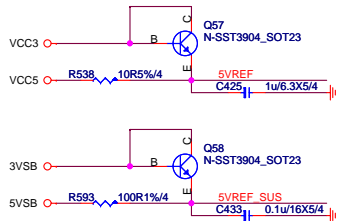
Size Custom	Document Description <b>PCH - SATA/ HOST/ DISPLAY</b>	Rev 3.1
Date: Friday, August 06, 2010		Sheet 9 of 31





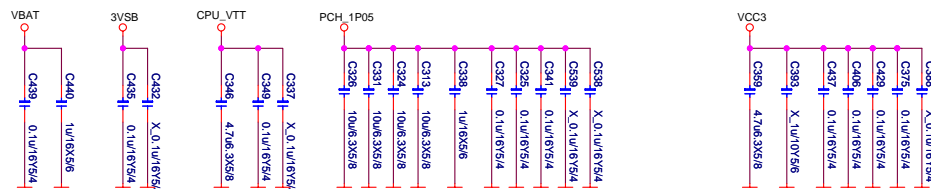
## 5VREF & 5VREF\_SUS Sequencing Circuit

5VREF must be powered up before VCC3 or after VCC3 within 0.7V.  
Also, 5VREF must power down after VCC3 or before VCC3 within 0.7V.  
This rule is also applies to 5VREF\_SUS and 3VSB.  
However, the 3VSB is derived from the 5VSB on the power supply  
thru a voltage regulator and therefore, they can satisfy the requirement.



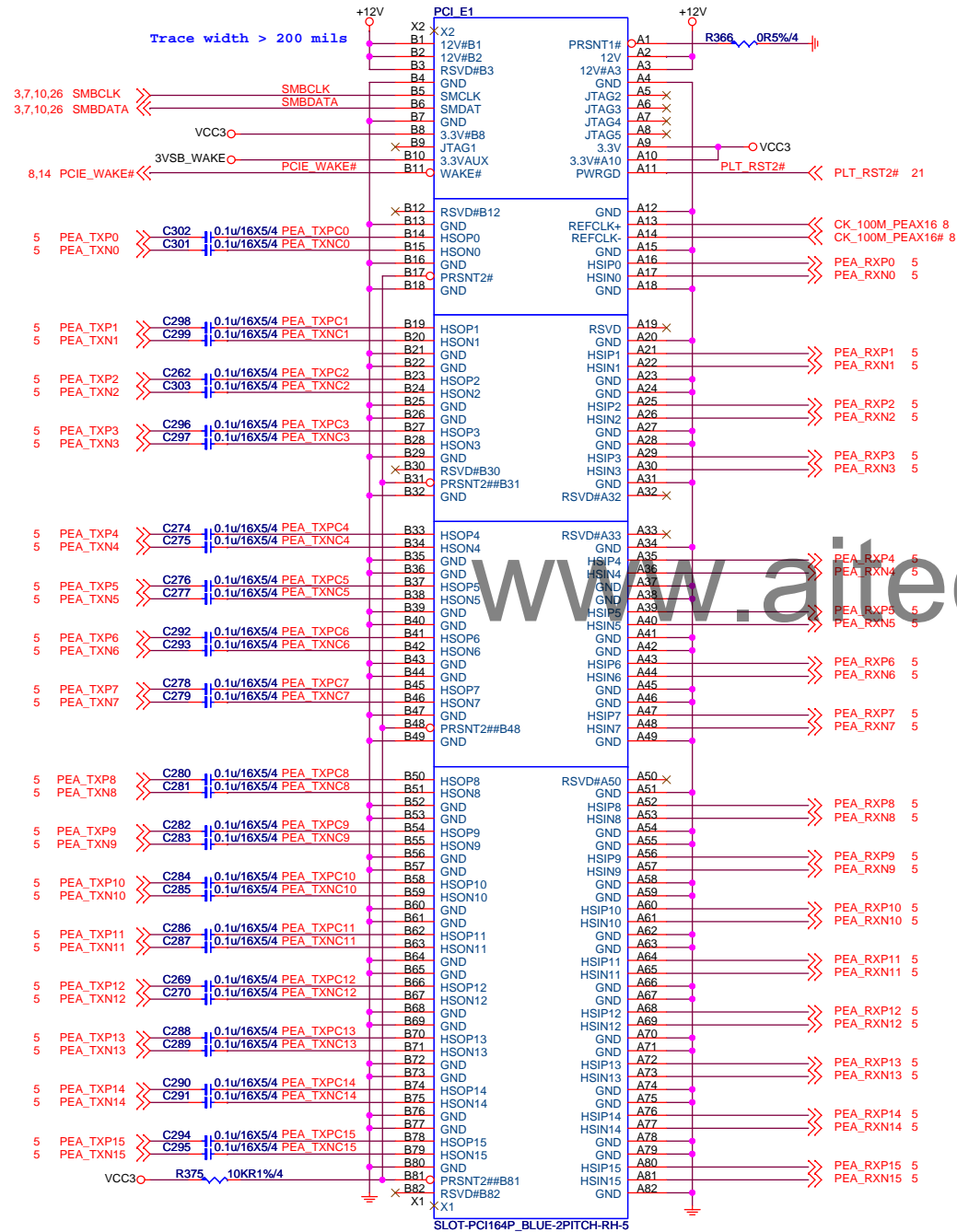
7 OF 9

## PCH decoupling cap

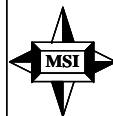
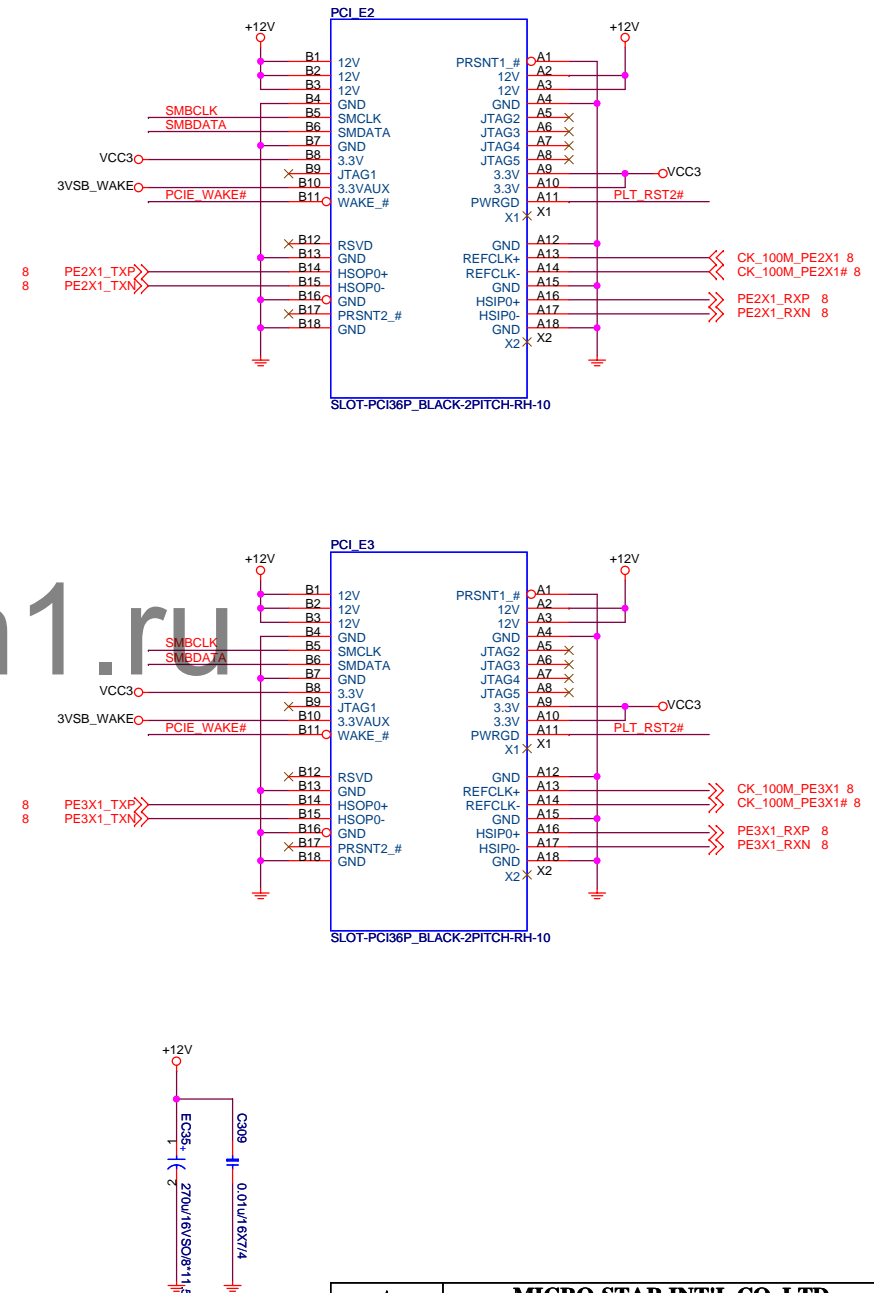




### PCI\_Express X16 Slot



### PCI\_Express X1 Slot



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Size Custom	Document Description <b>PCIE SLOT - X16 / X1</b>	Rev 3.1
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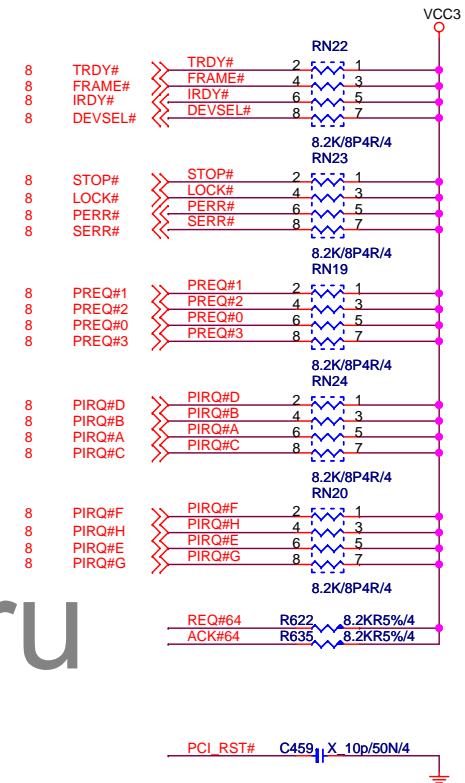
Date: Friday, August 06, 2010 Sheet 13 of 31





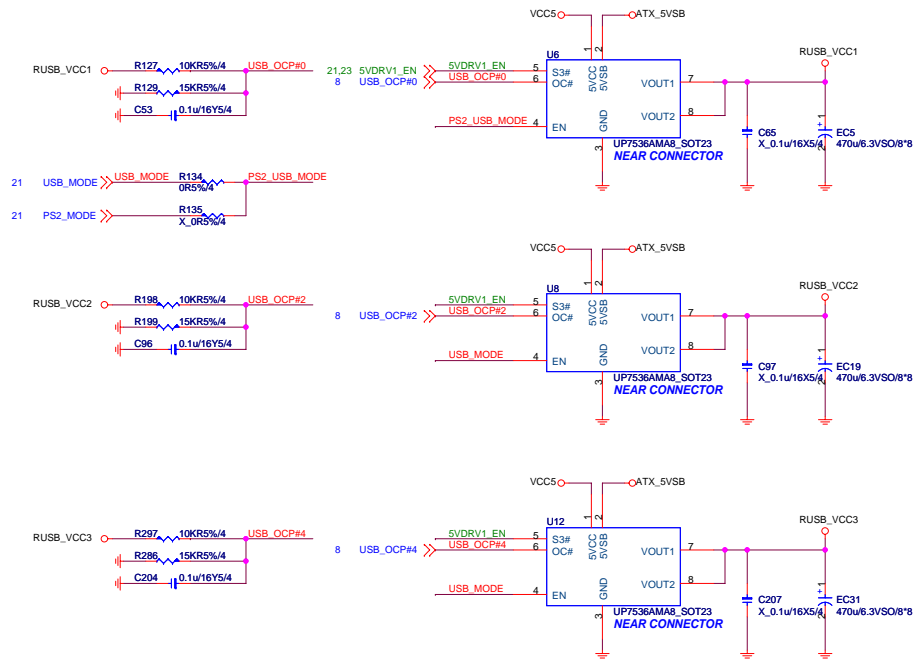


### PCI PULL-UP / DOWN RESISTORS

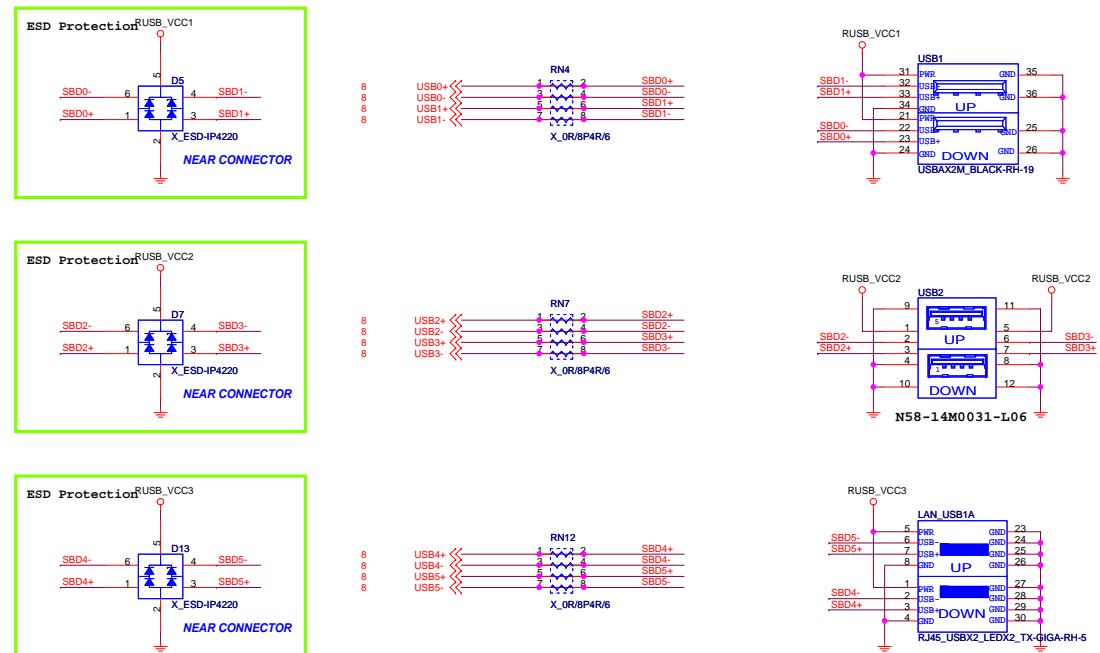
**MS-7636**

Size Custom	Document Description <b>PCI SLOT</b>	Rev 3.1
Date: Friday, August 06, 2010	Sheet 15 of 31	

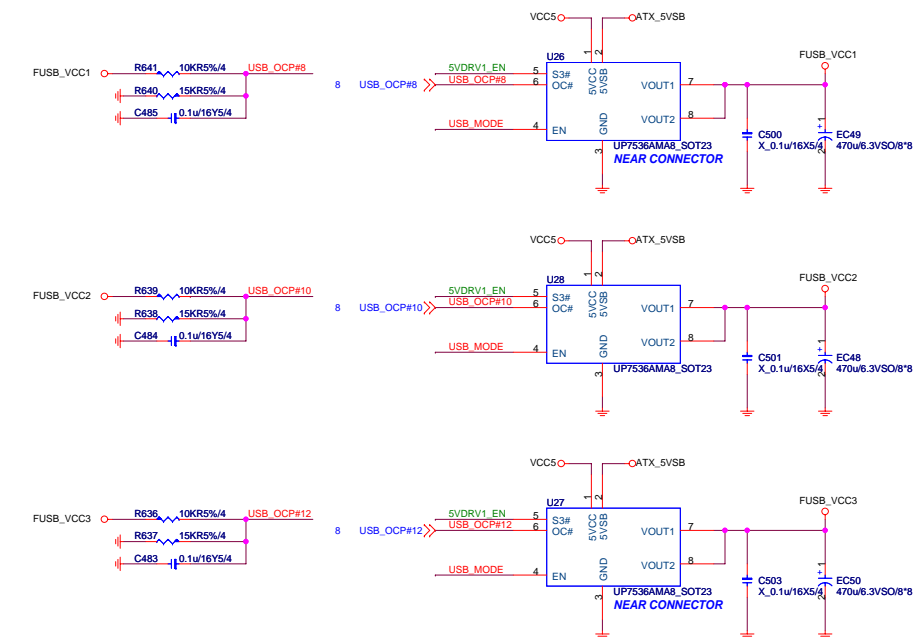
## POWER CIRCUIT FOR USB PORT 0 ~ 5



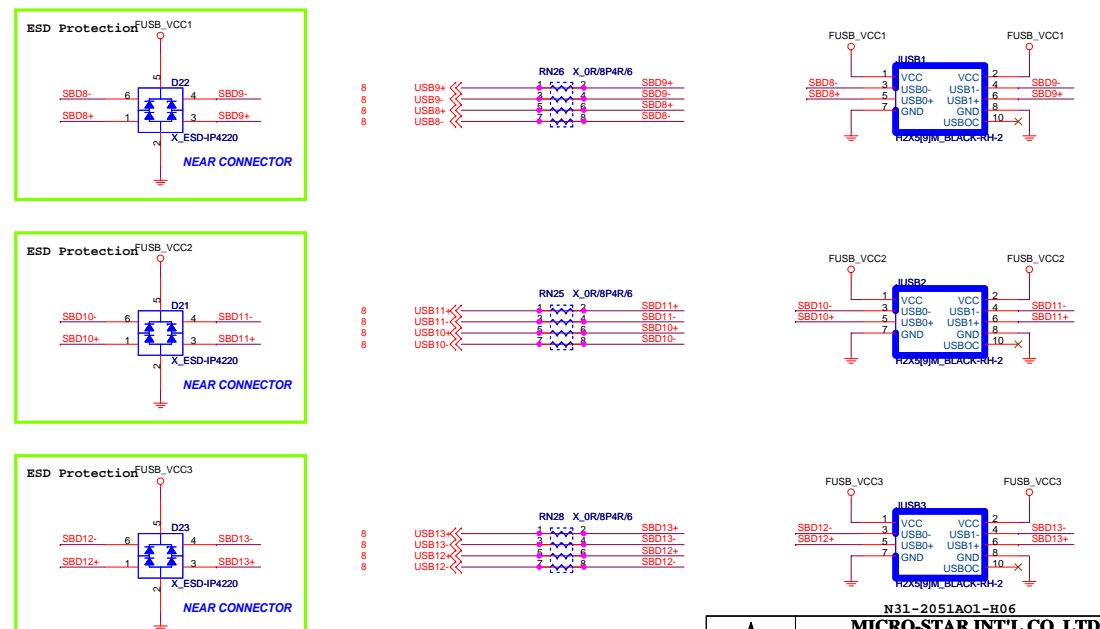
## REAR PANEL USB CONNECTOR FOR USB PORT 0 ~ 5



## POWER CIRCUIT FOR USB PORT 6 ~ 11

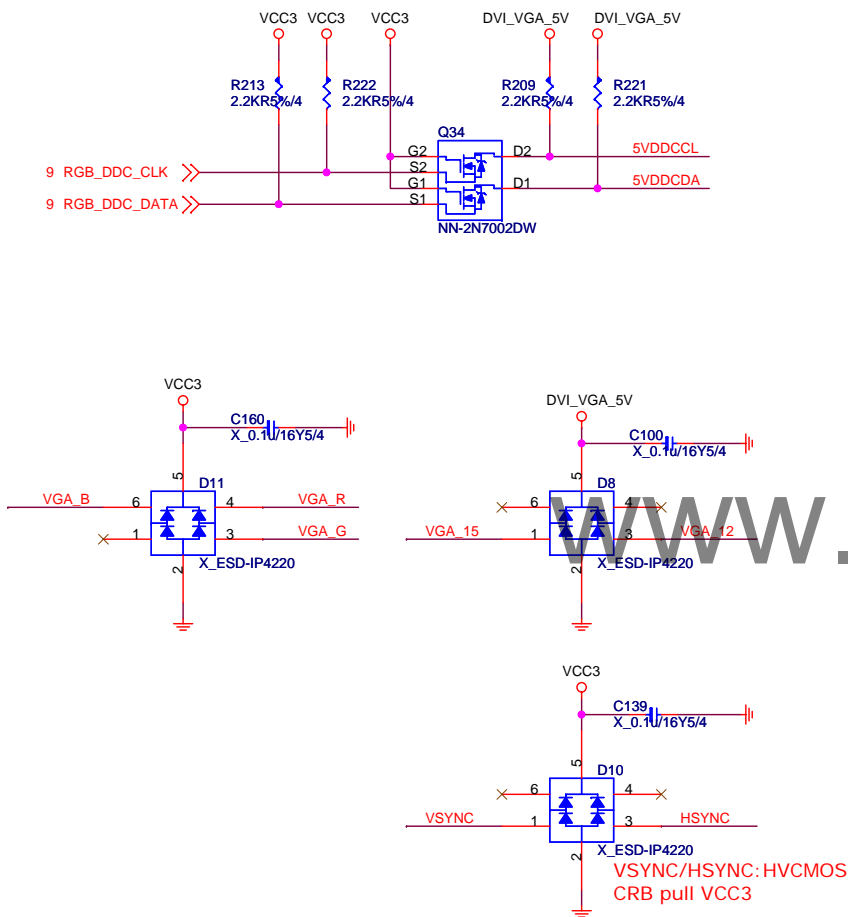


## FRONT PANEL USB CONNECTOR FOR USB PORT 6 ~ 11

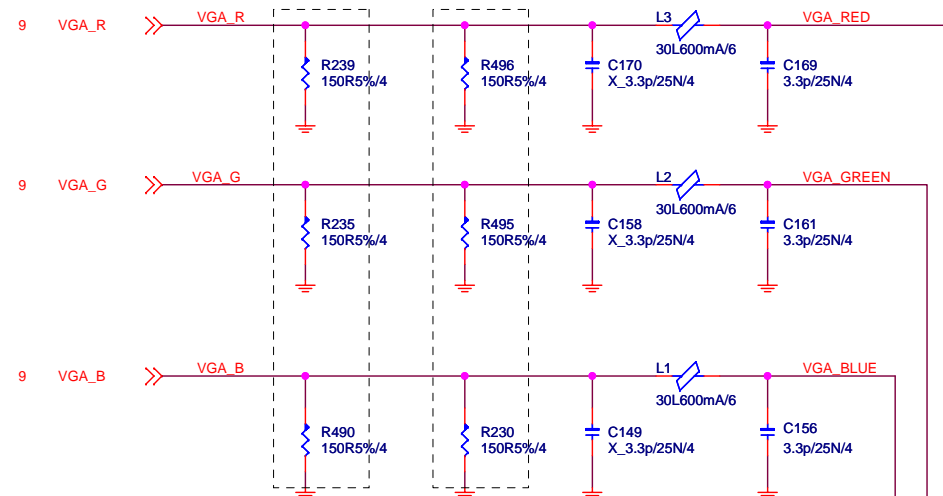


# D-Sub

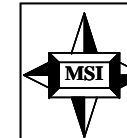
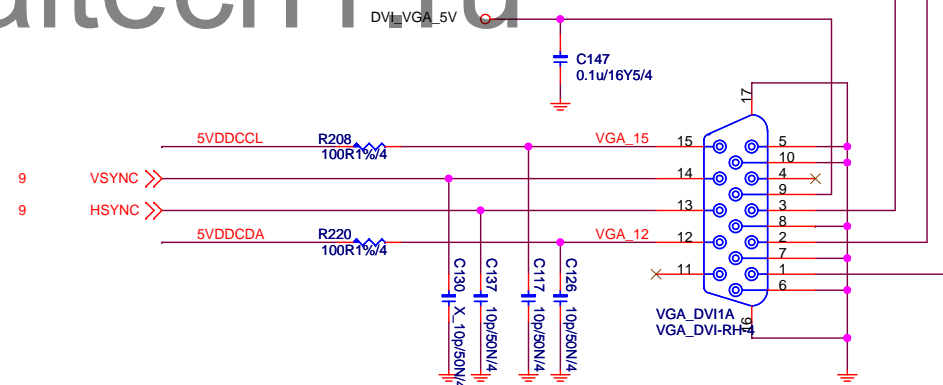
## Level shift



PLACE CLOSE TO VGA CONNECTOR,  
WITHIN 750 MIL OF PIN



Close to PCH within 250 mils.



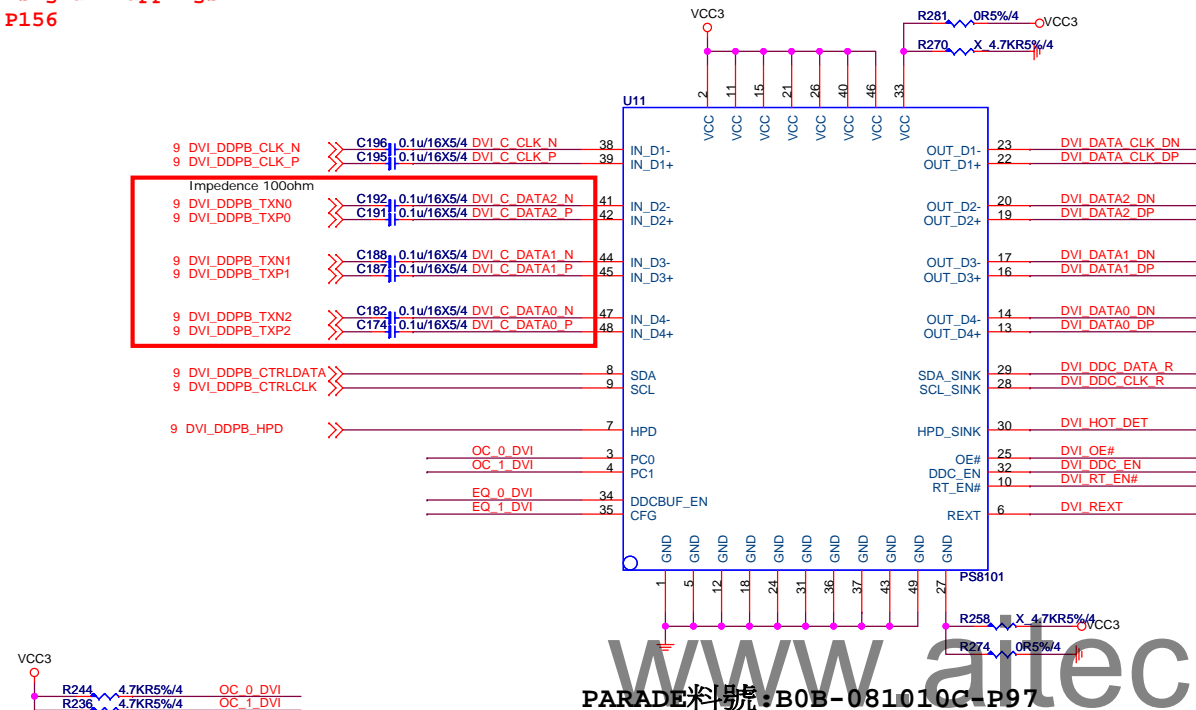
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Size Custom	Document Description VGA	Rev 3.1
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# DVI level shifter

PCH signal Mappings  
DG P156

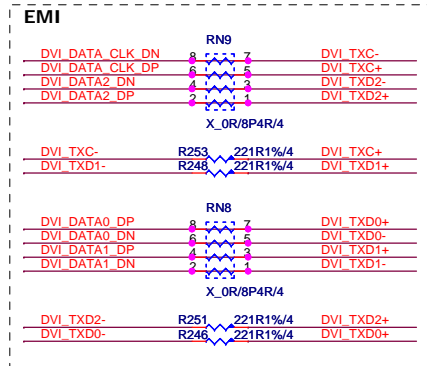
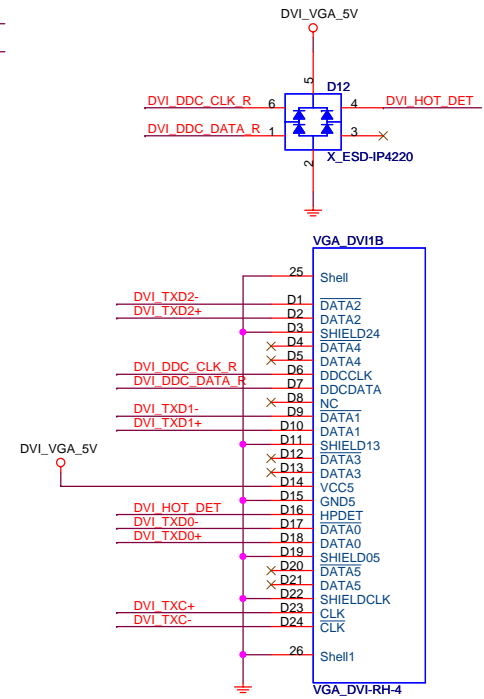
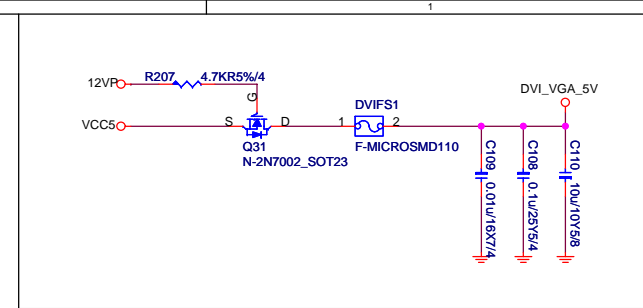
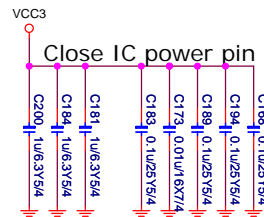
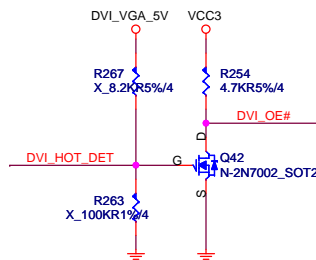
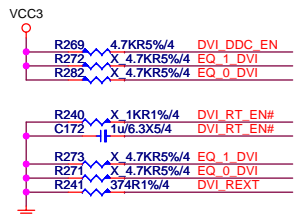


PC1	PC0	Internal pull-down at ~500K ohm	
0	0	8 dB	
0	1	4 dB	
1	0	12 dB	
1	1	0 dB	

PARADE料号: B0B-081010C-P97

DDC_EN, DDCBUF_EN, OE#	DDC Passive Switch	DDC Active Buffer
1, 0, X	On	Off
1, 1, 0	Off	On
1, 1, 1	Off	Off
0, X, X	Off	Off

	0	1	note
DDC_EN	DDC level shifter disable	DDC level shifter enable	Internal pull-up at ~500K ohm.
RT_EN#	Input 50 ohm termination resistor enable	the input termination resistors are set to high impedances the chip is power down and input termination resistors will be at high impedance.	Internal pull-down at ~500K ohm.
OE#	Enable	Enable	Internal pull-down at ~500K ohm.
HPD_SINK	Disable	Enable	Internal pull-down at ~200K ohm; 5V tolerant.
DDCBUF_EN	For DDC level shifting configuration, please refer to Table.		Internal pull-down at ~500K ohm.
REXT			analog current generation.



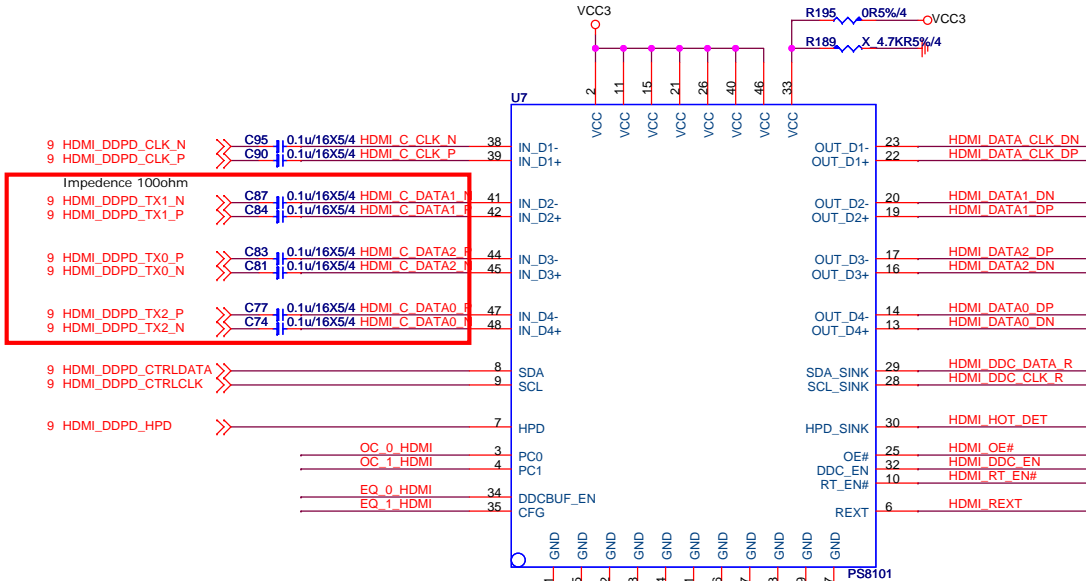
**MICRO-STAR INT'L CO.,LTD**

**MS-7636**

Size Custom Document Description **DVI - PARADE PS8101** Rev 3.1

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HDMI level shifter



VCC3

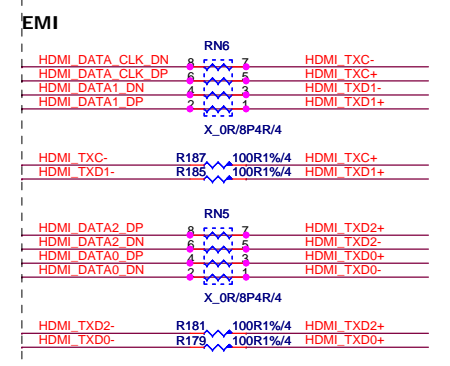
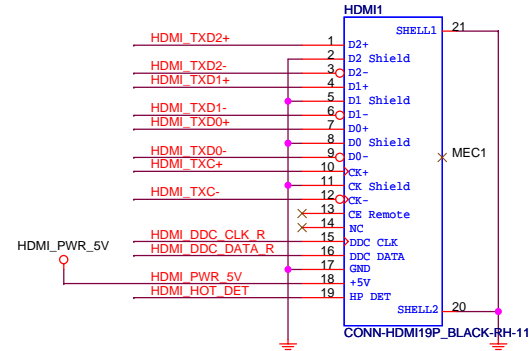
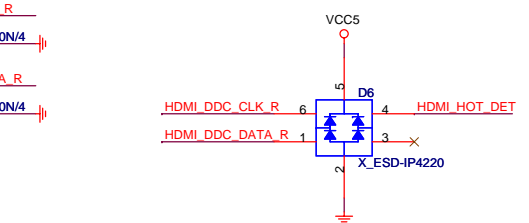
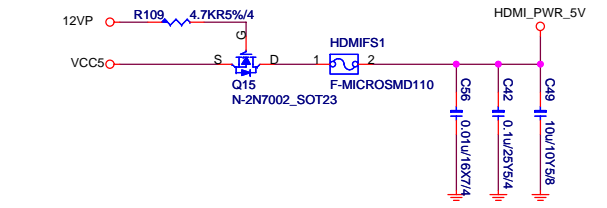
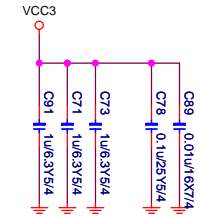
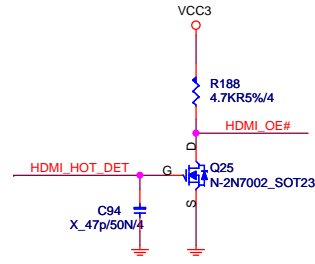
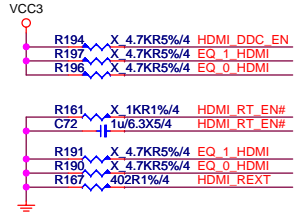
R163 4.7KR5%/4 OC 0 HDMI  
R162 4.7KR5%/4 OC 1 HDMI

R169 X 4.7KR5%/4 OC 0 HDMI  
R168 X 4.7KR5%/4 OC 1 HDMI

PC1	PC0	
0	0	8 dB
0	1	4 dB
1	0	12 dB
1	1	0 dB

DDC_EN, DDCBUF_EN, OE#	DDC Passive Switch	DDC Active Buffer
1, 0, X	On	Off
1, 1, 0	Off	On
1, 1, 1	Off	Off
0, X, X	Off	Off

	0	1	note
DDC_EN	DDC level shifter disable	DDC level shifter enable	Internal pull-up at ~500K ohm.
RT_EN#	Input 50 ohm termination resistor enable	the input termination resistors are set to high impedances the chip is power down and input termination resistors will be at high impedance.	Internal pull-down at ~500K ohm.
OE#	Enable	Enable	Internal pull-down at ~500K ohm.
HPD_SINK	Disable	Enable	Internal pull-down at ~200K ohm; 5V tolerant.
DDCBUF_EN	For DDC level shifting configuration, please refer to Table.		Internal pull-down at ~500K ohm.
REXT			analog current generation.



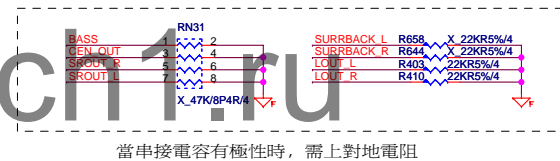
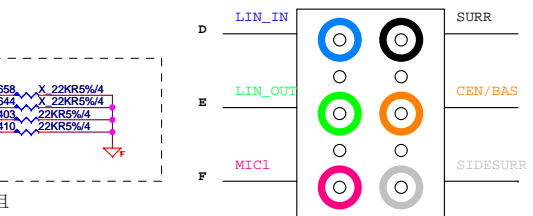
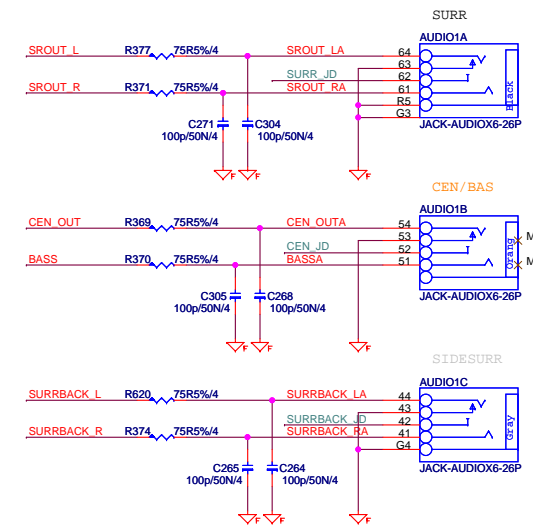
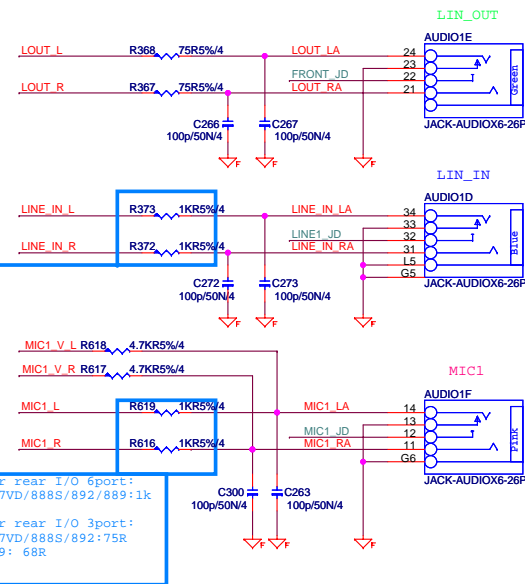
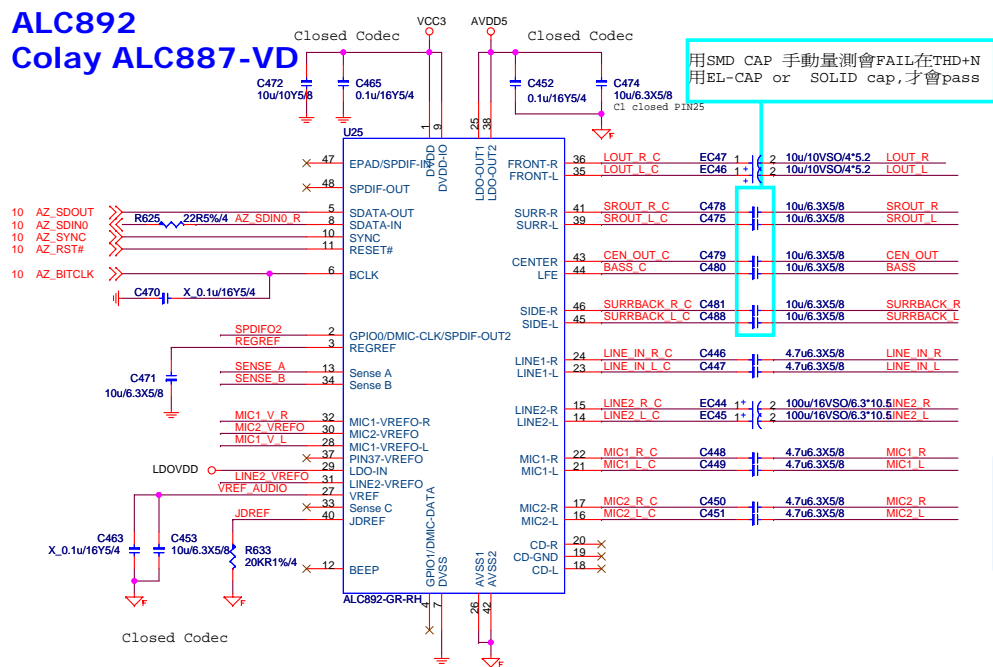
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**MS-7636**

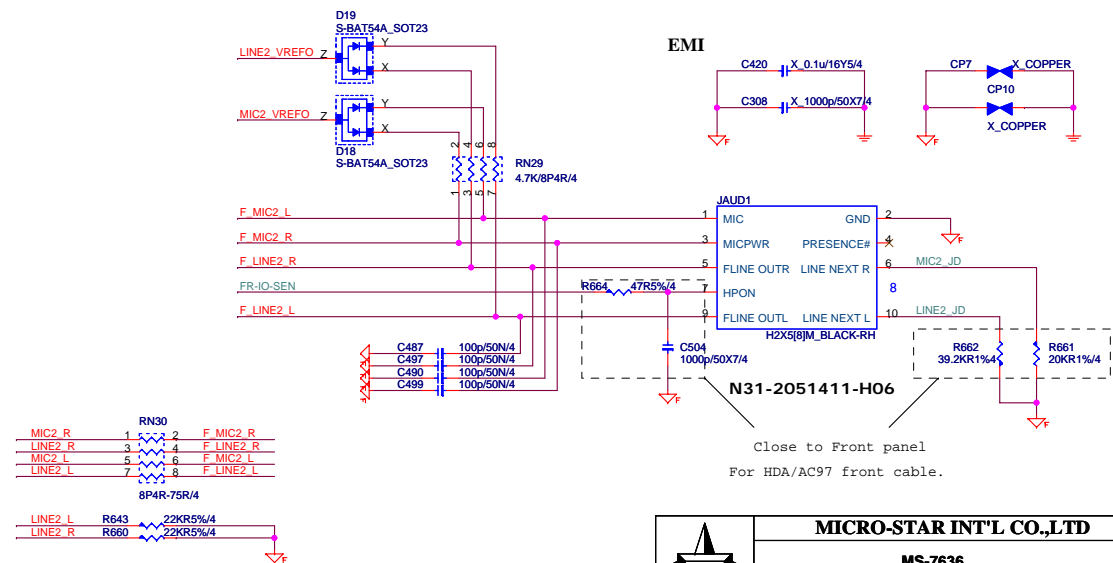
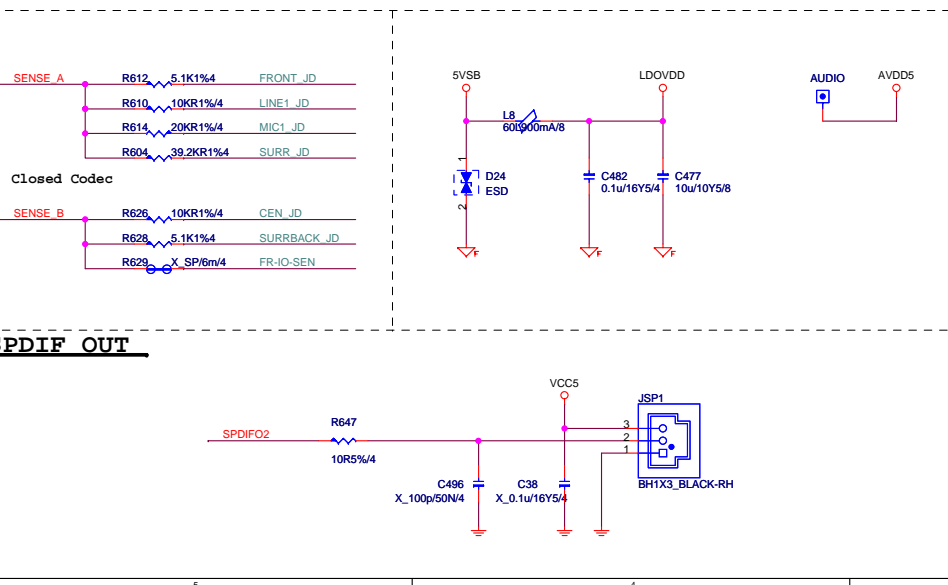
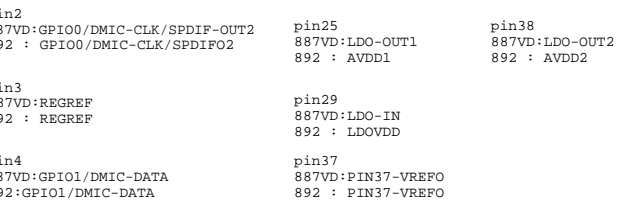
Size	Document Description	Rev
Custom	<b>HDMI - PARADE PS8101</b>	3.1

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ALC892  
Colay ALC887-VD

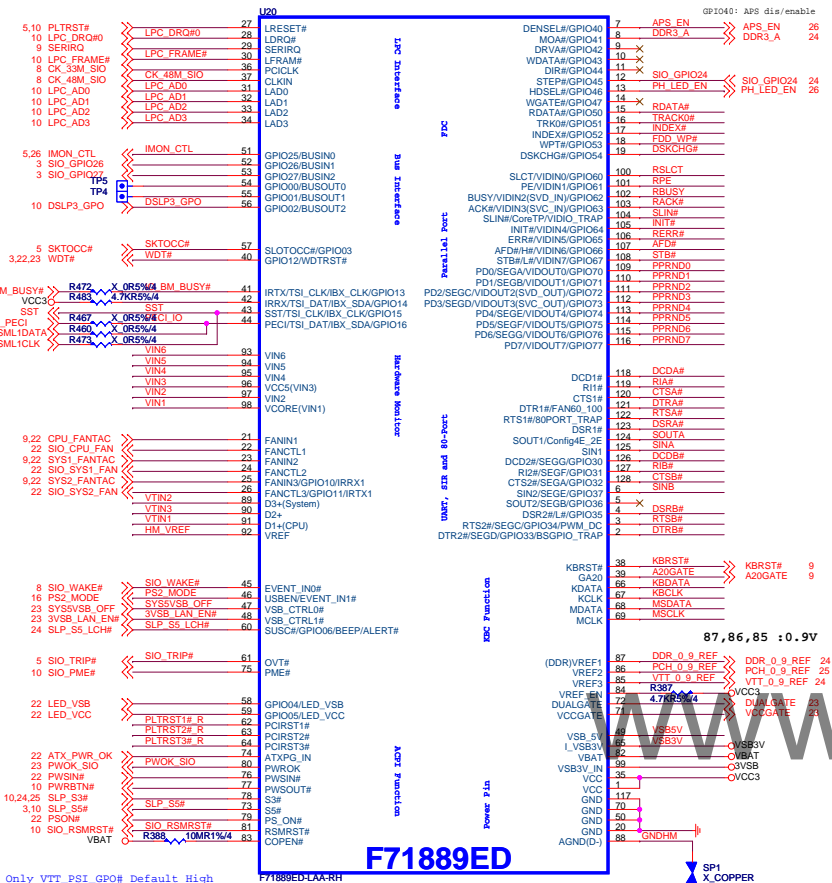


當串接電容有極性時，需上對地電阻



<b>MICRO-STAR INT'L CO.,LTD</b>			
<b>MS-7636</b>			
Size Custom	Document Description <b>Audio Codec - ALC889/ ALC 887</b>		Rev 3.1
Date: Friday, August 06, 2010		Sheet 20 of 31	

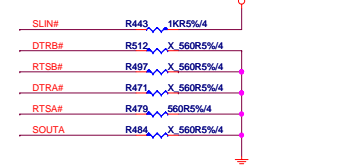




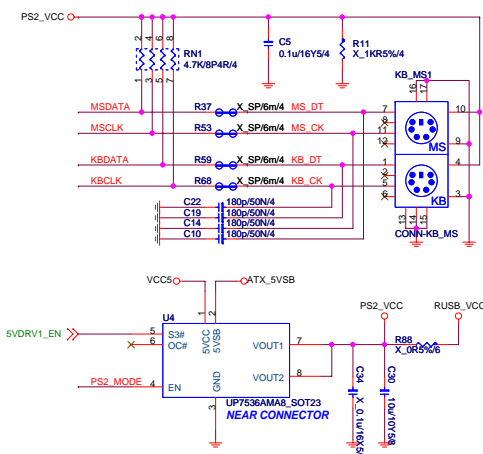
Only VTT\_PSI\_GPO# Default High  
Others Default Low

Strapping RESISTOR & Others Pull Hi Resistor

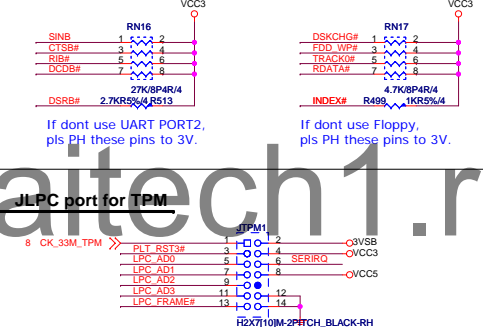
Don't STUFF	STUFF
SLIN#	Pull high 1k Pin 100-116 as LPT interfaces
DTRB#	PIN 51-56 = GPO
RTSB#	PIN 51-56 = BUS
PWM_FAN	LINEAR FAN
DTRA#	FAN START DUTY 60%
RTSA#	FAN START DUTY 100%
SOUTA	80 PORT ENABLE
	80 PORT DISABLE
	CONFIG 4E
	CONFIG 2E



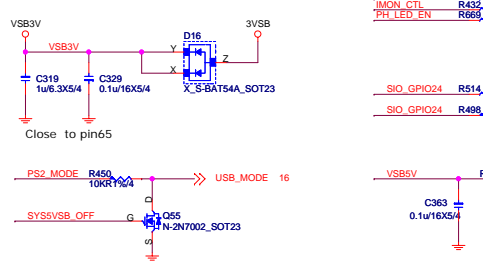
PS2 KEYBOARD & MOUSE CONNECTOR



COM2 / FLOPPY BOLCK

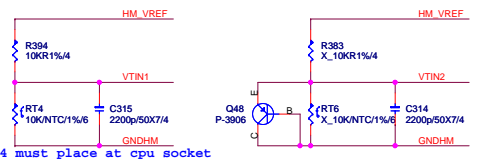


Eup CTL BLOCK

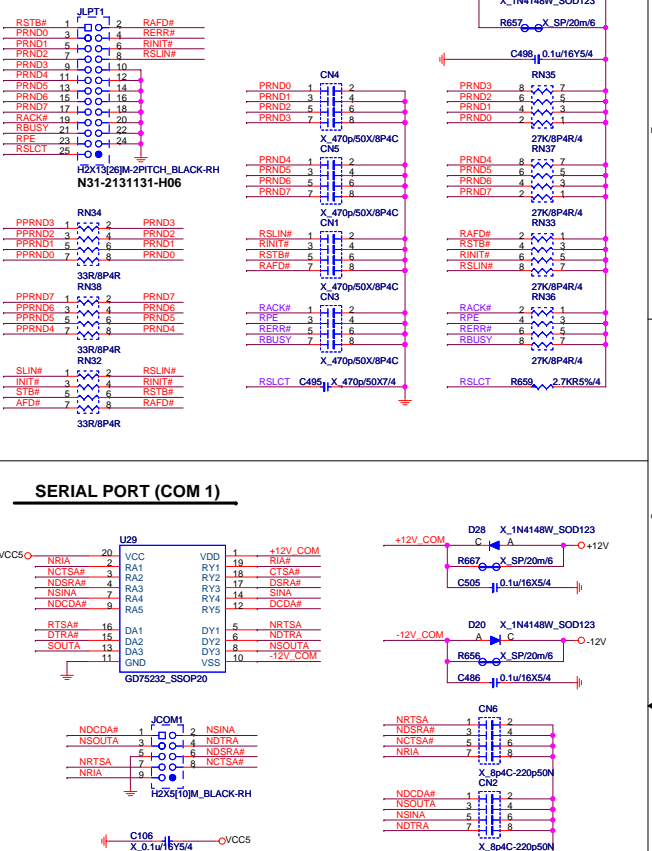


Temperature Sensing

Diode / Resistor SENSING CIRCUIT

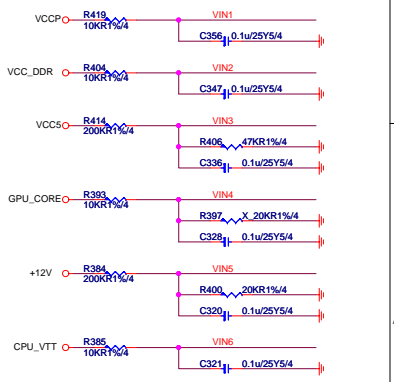


PARALLAL PORT



VOLTAGE SENSING(H/W Monitor)

The best voltage input level is about 1V.



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Size Custom | Document Description **SIO - F71889ED/ COM/ LPT/ TPM** | Rev 3.1

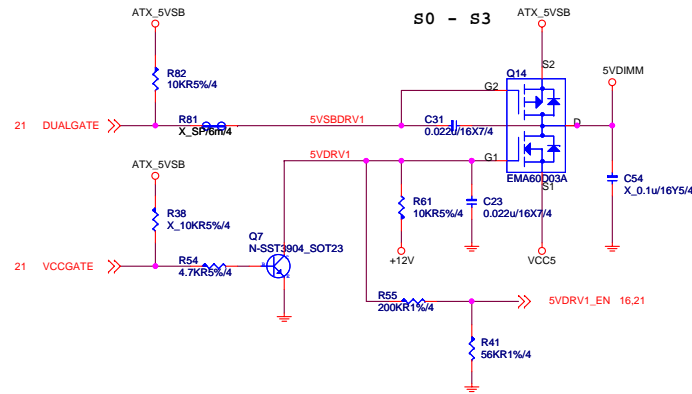
Date: Friday, August 06, 2010 | Sheet 21 of 31

Size Custom	Document Description <b>ATX CNT/ Front Panel/ FAN CTRL</b>	Rev 3.1
Date: Friday, August 06, 2010		Sheet 22 of 31

## 5VDDIMM

S0 - S3

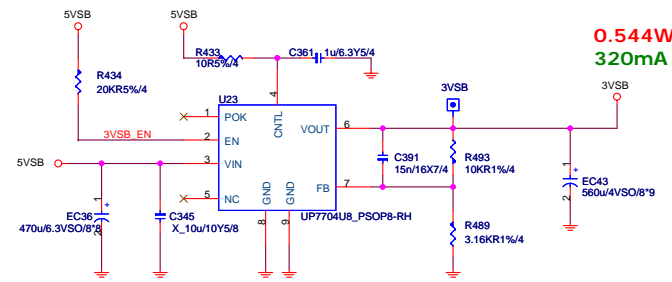
For DDR, 6.581A



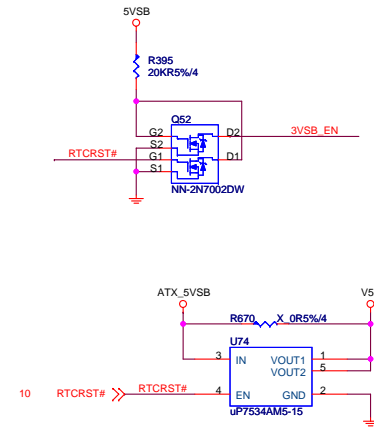
## 3VSB

S0 - S5

For PCH, 320mA



0.544W  
320mA

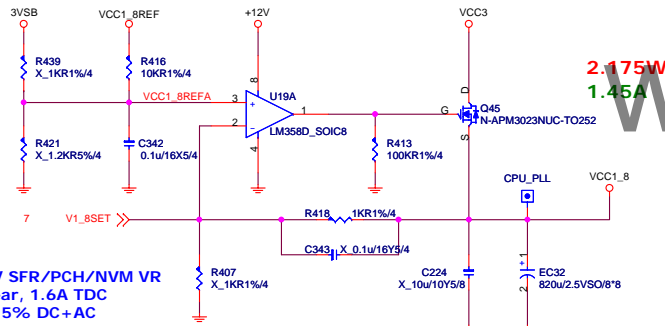


## VCC1\_8

S0

For CPU SFR, 1.35A

For PCH PLL, 0.1A



2.175W  
1.45A

1.8V SFR/PCH/NVM VR  
Linear, 1.6A TDC  
+/- 5% DC+AC

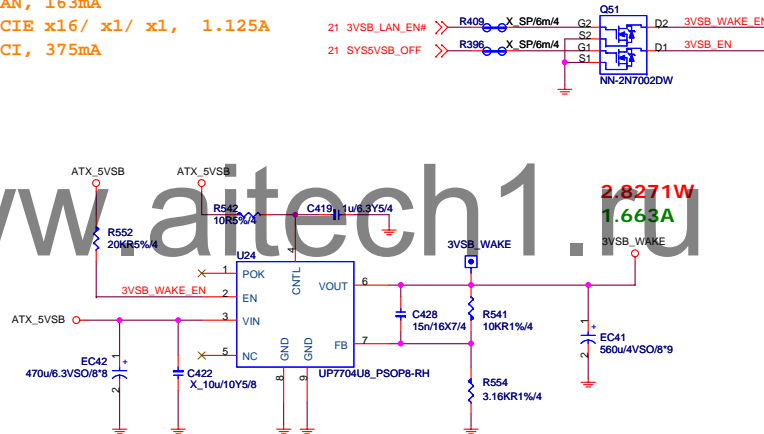
## 3VSB\_WAKE

S0 - S5

For LAN, 163mA

For PCIE x16/ x1/ x1, 1.125A

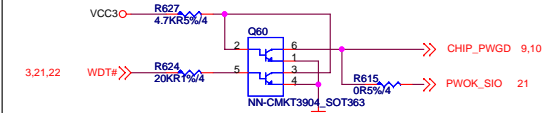
For PCI, 375mA



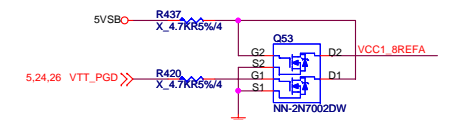
2.8271W  
1.663A

## PWROK DELAY

VID before PWROK > 3ms

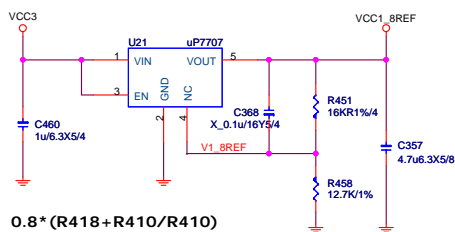


## cpvtt & pch vore wait 1.8v



## VCC1\_8REF

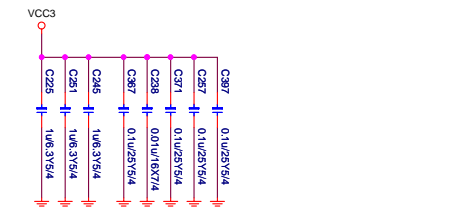
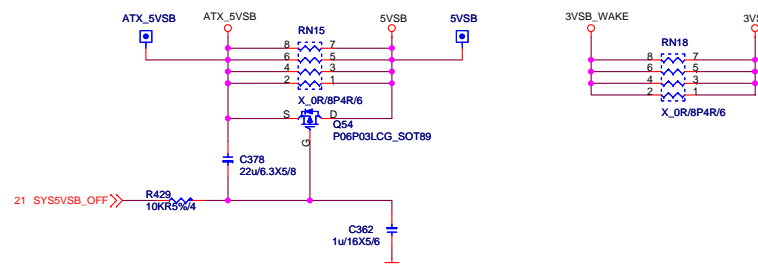
S0



0.8\* (R418+R410/R410)

## 5VSB Power Switch

Trace Width 80mils.



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Size Custom Document Description ACPI controller UPI Rev 3.1  
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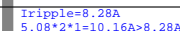
S0 - S3



19.5A  
29.25W

## VTT DDR:0.75A

0.75A  
0.562W



SO

35A)



35A  
38.5W

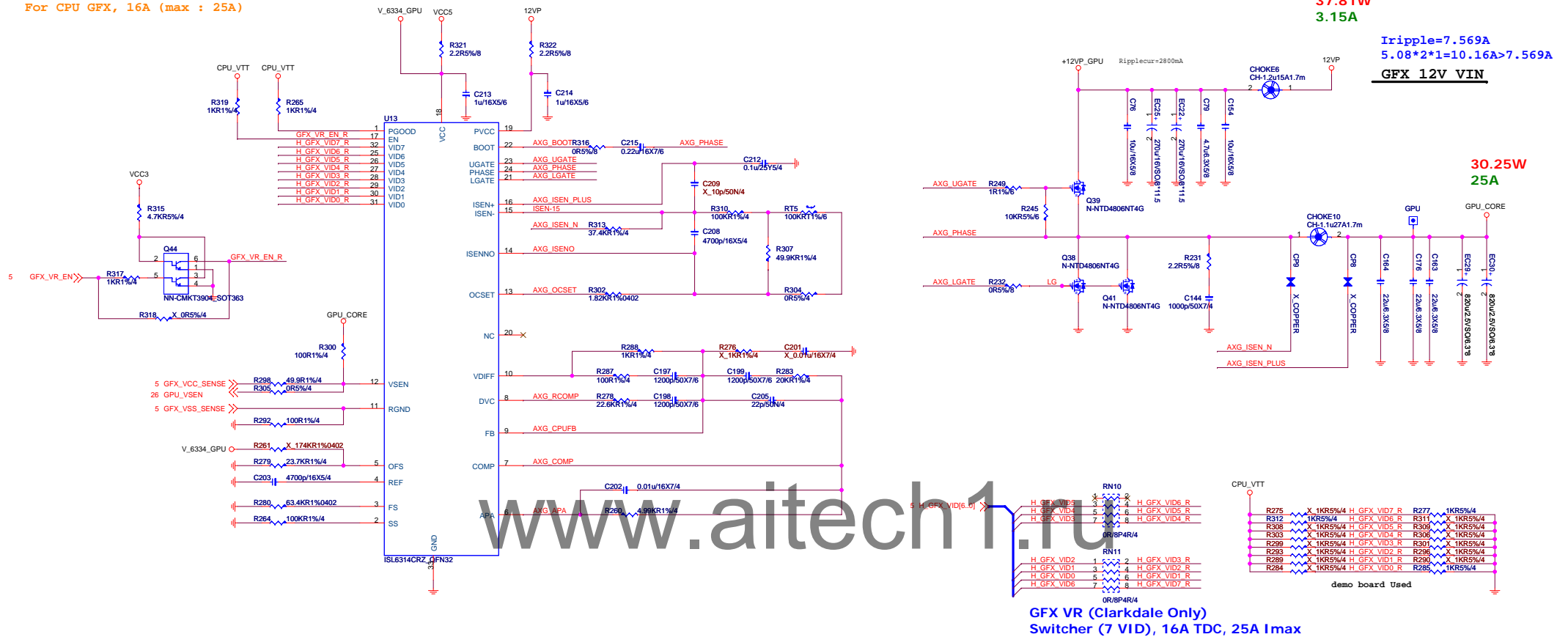
## 5,23,20



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Size Custom	Document Description <b>DDR POWER - UPI6103_1-Phase</b>	Rev 3.1
Date: Friday, August 06, 2010		Sheet 24 of 31

For CPU GFX, 16A (max : 25A)



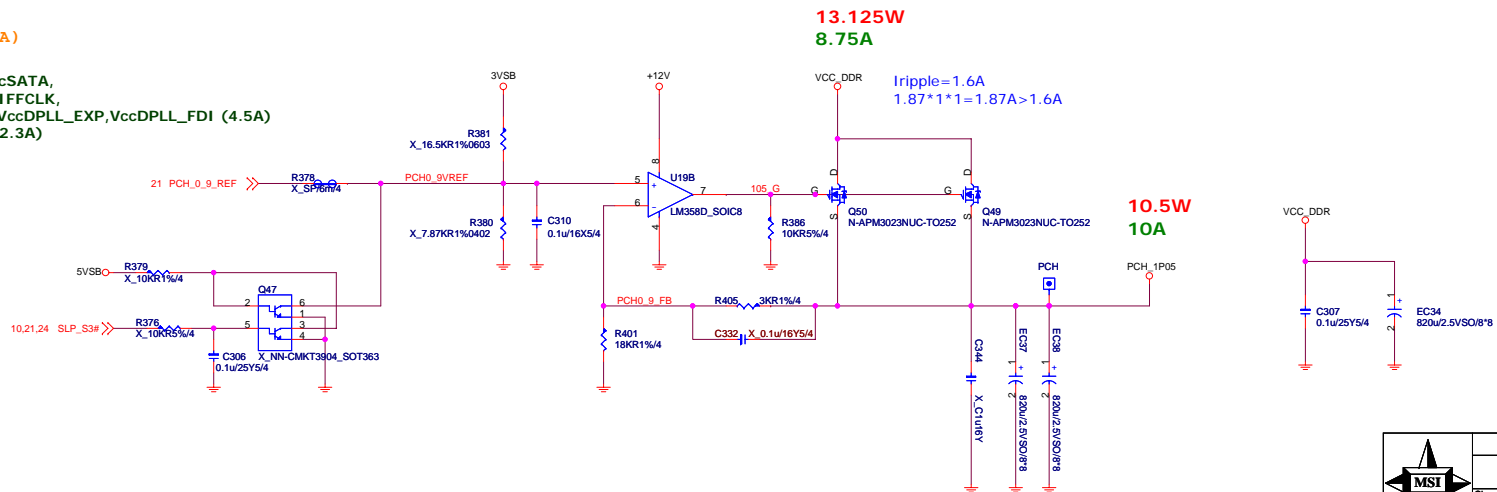
For PCH CORE, 4.5A (max : 7.5A)

For PCH ME, 2.3A (max : 2.5A)

### V1.05PCHS0: Vcc, VccExp, VccDMI, Vc

**V1.05PCHS0: Vcc, VccExp, VccDMI, VccSATA,  
VccSATAPLL, VccAUPLL, VccSSC, VccDIFFCLK,  
VccDIFFCLKN, VccUSB0RE, VccDPLL, VccDPLL\_EXP, VccDPLL\_FDI (4.5A)  
V1.05MEM: VccMEW, VccAUX, VccME (2.3A)**

### V1.05MEM: VccMEW, VccAUX, VccME (2.3A)



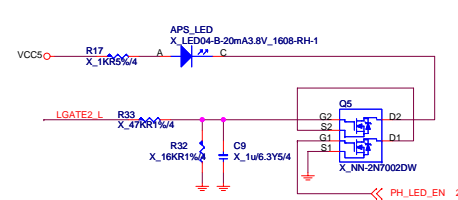
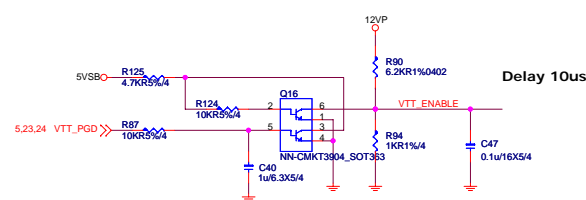
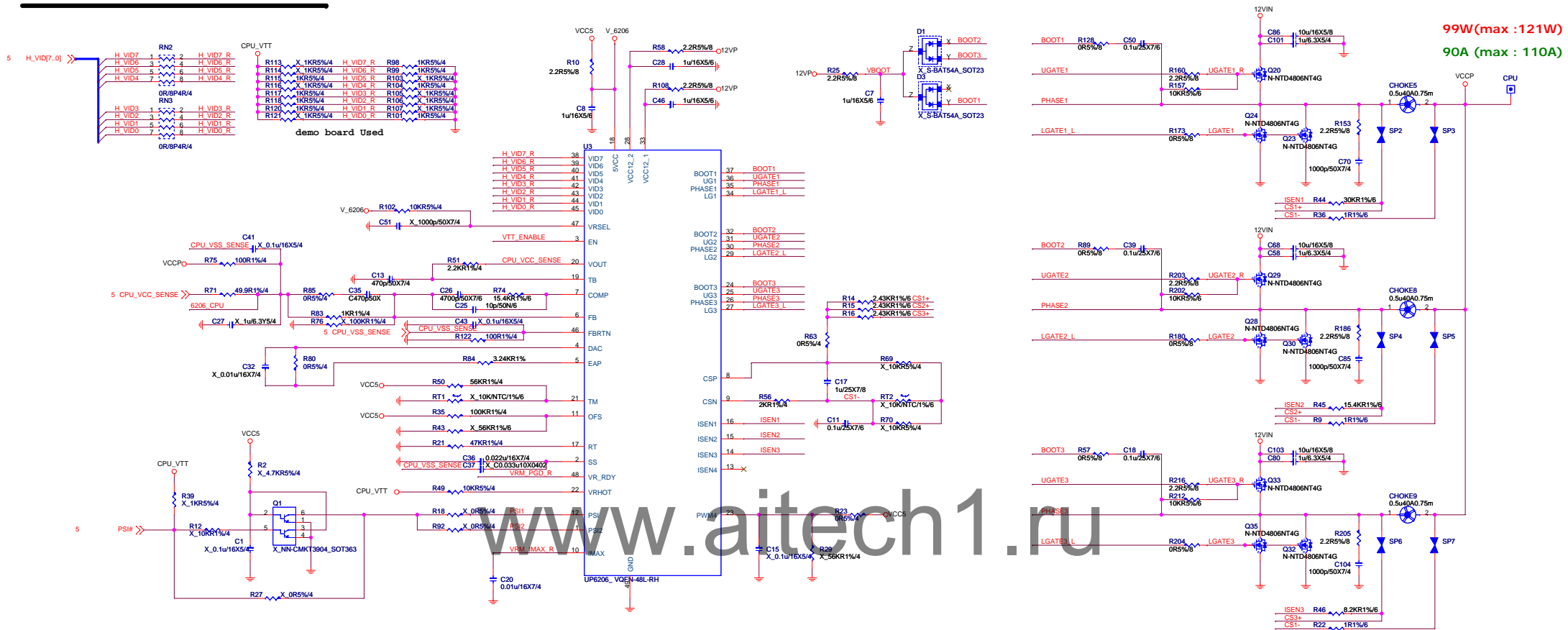
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Size	Document Description
Custom	<b>GPU PowerISL6117_1-Phase</b>

### 3.1

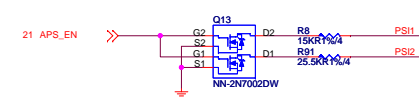
## Up6206 VRD11.1 POWER



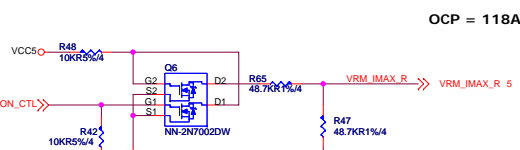
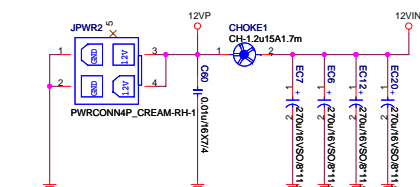
```

Enable PSI function
PSI Enable: 1 Phase          1->2 = 11.7A
PSI Disable: 3 Phase         2->3 = 25.5A

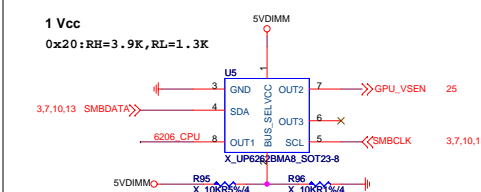
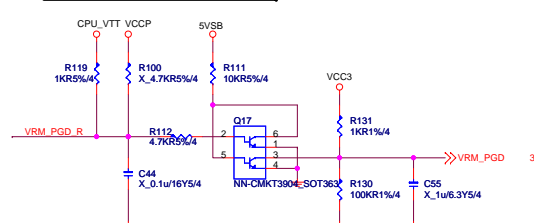
```



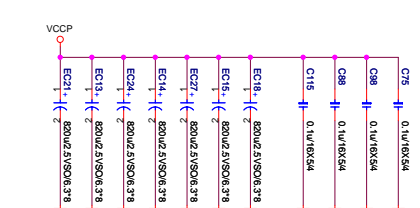
$I_{ripple} = 17A$   
 $5.08 * 4 * 1 = 20.32A > 17A$



## VRMPWRGD LEVEL SHIFT



Address	0x2A	0x28	0x26	0x24	0x22	0x20
R1 (kΩ)	open	3.9	3	2.2	1.3	10
R2 (kΩ)	10	1.3	2.3	3	3.9	open
BUS_SEL Voltage (% of VCC)	0	25	40	60	75	100



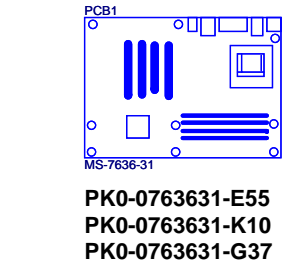
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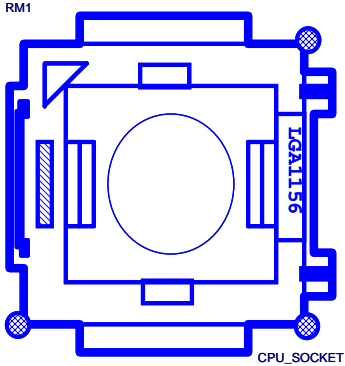
Size Custom	Document Description <b>VRD11.1 - nPI 6206_3-Phase</b>	Rev 3.1
Date: Friday, August 06, 2010		Sheet 26 of 31



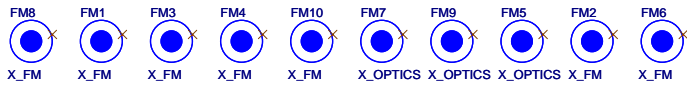
PCB



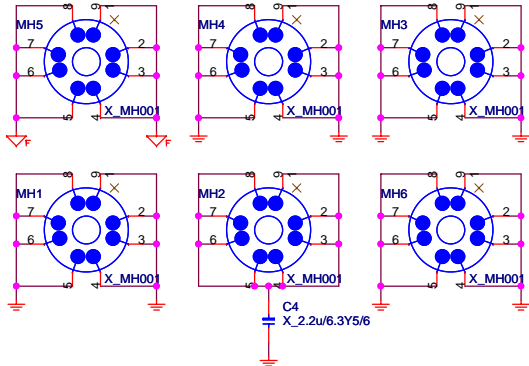
CPU SOCKET



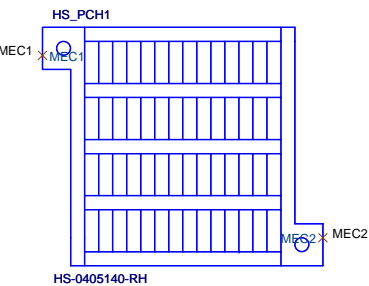
Optical Fiducial Marks-120



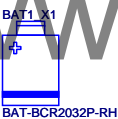
Mounting Holes



HEATPIPE



BATTERY



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Simulation

